AMENDMENT TO THE CLAIMS

1-6. (Canceled)

7. (Currently amended) A processor comprising:

an instruction register which stores two instructions;

a decoder which decodes the two instructions;

a first execution unit;

a second execution unit; and

instruction parallelizing/executing means for executing the two instructions, which designate the first execution unit as a target, in parallel by allocating one of the two instructions to the second execution unit,

wherein the parallelizing/executing means is [[capable of converting]] configured to convert one of the two instructions to another equivalent instruction that designates the second execution unit.

8. (Previously presented) The processor of claim 7, wherein the parallelizing/executing means comprises:

instruction recognizing means for recognizing the two instructions as instructions both designating the first execution unit as the target;

allocation changing means for converting one of the two instructions to another equivalent instruction that designates the second execution unit and reallocating said another instruction to the second execution unit; and

parallel executing means for executing the two instructions in parallel.

9-10. (Canceled)

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